# U23ITT31-COMPUTER ORGANIZATION AND ARCHITECTURE

## PART A & PART B

## UNIT 1-OVERVIEW & INSTRUCTION

## PART A

1. **List the registers that are available in the processor?(Nov/Dec 2019)**

   **Registers are built from fast multi-ported memory cell. There are various types of Registers those are used for various purpose. Some Mostly used Registers are Accumulator(AC), Data Register(DR), Address Register(AR), Program Counter(PC), Memory Data Register (MDR), Index Register(IR), Memory Buffer Register(MBR).**

2. **State and explain the performance equation?(Nov/Dec 2019)**

   **Suppose that the average number of basic steps needed to execute one machine instruction is S, where each basic step is completed in one clock cycle. If the clock cycle rate is R cycles per second, the program execution time is given by T = (N x S) / R This is often referred to as the basic performance equation.**

3. **Define Computer Architecture.**

   **Computer Architecture deals with the structure and behavior of a computer including the information formats.**

4. **Define processor clock and clock rate**

   Processor clock: Processor circuits are controlled by a timing signal called processor clock, the clock defines regular time interval called clock cycle. Clock Rate: Clock rate, R=1/p cycles/sec(hz) Where p is length of one clock cycle

5. **Define word length? (NOV/DEC 2011)**

   Each group of n bits is referred to as a word of information and n is called the word length.

6. **Explain the relation of throughput with execution and response time**

   Throughput: The total amount of work done in a given time

   Let us consider 2 cases:

   1.) Replacing the processor in a computer with a faster version

   2.) Adding additional processor to a system that uses multiple processors for

separate task. Ex: Handling an airline reservation systems.

Decreasing response time almost always improves throughput. So, in case 1 both response time & throughput increases. In case2 none of the task gets work done faster, so throughput increases. However, the demand for processing in the 2nd case was almost as large as the throughput, the system might force requests to queue up. In this case increasing the throughput could also increase the response time, since it would decrease the waiting time in queue. Thus many real computer systems, changing either execution time or throughput often affects the other.

**7. Define MIPS Rate and Throughput Rate**.

MIPS: **One alternative to time as the metric is MIPS(Million Instruction Per Second)**

**MIPS=Instruction count/(Execution time x1000000). This MIPS measurement is also called Native MIPS to distinguish it from some alternative definitions of MIPS.**

**MIPS Rate: The rate at which the instructions are executed at a given time.**

**Throughput: The total amount of work done in a given time.**

**Throughput rate: The rate at which the total amount of** work done at a given time.

**8. What is MFLOPS? What is its significant?**

Popular alternative to execution time is Million Floating-point Operations Per Second , abbreviated megaflops orMFLOPS but always pronounced "megaflops".The formula for MFLOPS is simply the definition of the acronym: MFLOPS=Number of floating-point operations in a program/(Execution timex1000000).

A MFLOPS rating is dependent on the program.Different programs require the execution of different number of floatin point operations.Since MFLOPS were intended to measure floating-point performance,they are not applicable outside that range.Compilers,as an extreme example,have aMFLOPS rating near 0 no matter how fast the machine is,because compilers rarely use floating-point arithmetic.

**9. Define CPI**

The term ClockCyclesPerInstruction Which is the average number of clock cycles each instruction takes to execute, is often abbreviated as CPI. CPI= CPU clock cycles/Instruction count.

**10. State and explain the performance equation?**

Suppose that the average number of basic steps needed to execute one machine instruction is S, where each basic step is completed in one clock cycle. If the clock cycle rate is R cycles per second, the program execution time is given by T = (N x S) / R. This is often referred to as the basic performance equation.

**11. What do you mean by aligned and unaligned address?**

Aligned address: In the case of 32bit word length, natural word boundaries occur at address

0,4,8……the word locations have aligned address. In general, words are said to be aligned in memory if they begin at a byte address that is a multiple of the number of bytes in a word. FOR EXAMPLE: If the word length is 16(2bytes), aligned words begin at byte address 0, 2, 4

Unaligned address: There is no fundamental reason why words cannot begin at an arbitrary byte address. The words are said to have unaligned address. While the most common case is to use aligned address, some computers allow the unaligned word address

**12. What is the assembly language notation? Give example.**

To **represent machine instructions and program. we use assembly Language format.**

**For example: The statement specifies an instruction that causes the transfer described above, from memory location LOC to processor registerR1.**

**Move LOC, R1**

**The contents of LOC are unchanged by the execution of this instruction, but the old contents of register R1 are overwritten.**

**The second example of adding two numbers contained in processor registers R1and R2 and placing their sum in R3 can be specified by the assembly language Statement and the assembly language statement can specify R2 and placing their**

**Sum inR3.**

Add R1, R2, R3.

**13. What is straight –line sequencing?**

Process of fetching and executing an instruction; one at a time in order of Increasing address with the help of information in program counter.

**14. Specify the sequence of operation involved when an instruction is Executed.**

- **Instruction Fetch**
- **Instruction Decode**
- **Operand Fetch**
- **Execute**

**15. what are Condition Codes (CC)? Explain the use of them.**

**Condition Codes are the list of possible conditions that can be tested during Conditional instructions.CC is used to test the condition (<, =,>). Based on this result, Jump instructions move to specified loop.CC flags represent The value of processor that keeps the information about the results of various Operations** for use by conditional branches

**16. What are addressing modes?**

Ø The **different ways in which the location of an operand is specified in an Instruction is referred to as addressing modes.**

**Ø It is a rule for interpreting or translating addresses field of an instruction Into an effective address from where the operand is actually** referenced.

**17. Define absolute addressing?**

**Absolute addressing is defined as the operand is in a memory location. The Address of this location is given explicitly in the instruction. It may also called as Direct addressing.**

**Assembler syntax: LOC**

**Addressing function: EA=LOC**

**Where, EA=Effective address**

**18. Define index mode?**

Index mode is defined as the effective address of the operand is generated By adding a constant value to the contents of a register.

Symbolic Representation,

X(Ri)

Where, X is a constant value

Ri is the name of the register.

Addressing function,

EA=[Ri] +X

**19. What are Number Notations?**

When dealing with numerical values, it is often convenient to use the familiar decimal notation. These values are stored in the computer as binary numbers. In some situations it is more convenient to specify the binary patterns directly. Most assemblers allow numerical value to be specified in different ways.

**20. List out the methods used to improve system performance.**

The methods used to improve system performance are

- Pipelining
- Clock rate
- Instruction set
- Compiler

## PART-B

1 .i).Summarize the eight great ideas of computer Architecture. ii). Explain the technologies for Building Processors.(7)(6)

2. List the various components of computer system and explain with neat diagram.(13)

3 i).Define addressing mode. ii).Describe the basic addressing modes for MIPS and give one suitable example instruction to each categorY(4) (9) (NOV/DEC-2011) (MAY/JUNE-2011) (Nov/Dec 2019)

4. Examine the operands and operations of computer hardware. (13)

5.i).Discuss the logical operations and control operations of computer. ii). Express the concept of Powerwall processor. (7)(6)

6 . Describe the factor influncing performance. (NOV/DEC-2011)

7. Explain the performance of the computer. (APRIL/MAY-2010)

8.i).Formulate the performance of CPU. ii).Compose the factors that affect performance. (7) (6)

9.i). Compare uni-processors and multi- processors. ii). Analyze how instructions that involve decision making are executed with an example. (3) (10)

10.Analyze the various instruction formats and illustrate with an example. (13) (MAY/JUNE-2013)

## UNIT-2 ARITHMETIC OPERATIONS

## PART A

1. **What are the rules to perform addition on floating point numbers? (Nov/Dec 2019)**
   - Choose the number with the smaller exponent and shift its mantissa right a Number of steps equal to the difference in exponents.
   - Set the exponent of the result equal to the larger exponent.
   - Perform addition /subtraction on the mantissa and determine the sign of the Result.
   - Normalize the resulting value, if necessary.

2. **What is sub word parallelism? (Nov/Dec 2019)**

   In subword parallelism, multiple subwords are packed into a word and then process whole words. A subword is a lower precision unit of data contained within a word. … Since the same instruction is applied to all subwords within the word, This is a form of SIMD(Single Instruction Multiple Data) processing

3. **Define the following terms. i. Overflow ii.Underflow**

   Overflow: In the single precision, if the number requires a exponent greater then +127 Or in a double precision, if the number requires an exponent form the overflow Occurs.

   Underflow: In a single precision ,if the number requires an exponent less than -26 or in a Double presition,if the number requires an exponent less than -1022 to represent Its normalized form the underflow occurs.

4. **What is the principle of booth multiplication?**

   Booth multiplication is nothing but addition of properly shifted multiplicand Patterns. It is carried out by following steps:

   - Start from LSB. Check each bit one by one.
   - Change the first one as -1.

- Skip all exceeding one‟s (record them as zeros) till you see a zero. Change this Zero as one.
- Continue to look for next one without disturbing zeros, precede using rules b), And c)

5. **List out rules for Booth recoded multiplier?**
   - Start from LSB check each bit one by one.
   - Change the first one as -1.
   - Skip all succeeding ones (record them as zero‟s) until you see a zero, Change this zero as one.
6. **List out rules for Booth recoded multiplier?**
   - Start from LSB check each bit one by one.
   - Change the first one as -1.
   - Skip all succeeding ones (record them as zero‟s) until you see a zero, Change this zero as one.
7. **List out the rules for mul /div of floating point number?**

   Multiply rule: Add the exponent and subtract 127, Multiply the mantissa and determine the sign of the result. Normalise the resulting value, if necessary.

   Divide rule: Subtract the exponents and add 127, Divide the mantissa and determine the sign of the result, Normalise the resulting value, if necessary.

8. **Write short notes on?**
   - Guard bits.
   - Truncation.
9. **Define Overflow**

   Overflow: In the single precision, if the number requires a exponent greater then +127 Or in a double precision, if the number requires an exponent form the overflow Occurs.

10. **Define Underflow**

    Underflow: In a single precision ,if the number requires an exponent less than -26 or in a Double prediction, if the number requires an exponent less than -1022 to represent Its normalized form the underflow occurs.

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    - Skip all exceeding one’s (record them as zeros) till you see a zero. Change this Zero as one.
    - Continue to look for next one without disturbing zeros, precede using rules b), And c)

12. **Convert the following binary numbers into booth recorded form.**
    - 1)11010 Booth recorded form =0-11-10
    - 2)14 Booth recorded form=100-10.
13. **List the two techniques used for speeding up the multiplication process:**

The two techniques used for spreading up the multiplication process are

- 1)Bit pair recording or modified Booth algorithm
- 2) Carry save addition of summands.

**14. What are the advantages of Booth algorithm?**

- It handles both positive and negative multipliers uniformly.
- It achieves some efficiency in the no. of additions required when the multiplier has a few large blocks of 1‟s.
- The speed gained however by skipping over 1's depends on the data.

15. **Write format for floating point in IEEE single–precision format**.

0 10001000.0010110…..

Value Represented = +0.0010110.x29

- UnNormalized Version

0 10000101. 0110… 26

- Normalized Version

**16. Define n-bit ripple-carry adder.**

A cascaded connection of n full adder blocks can be used to add two n-bit Numbers. Since the carries must propagate or ripple, through the cascade, the Configuration is called n b-bit ripple carry adder.

17. **How can we speed up the multiplication process?(CSE Nov/Dec 2003)**

There are two techniques to speed up the multiplication process:
1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands
2) The second technique reduces the time needed to add the summands.

**18. Why floating point number is more difficult to represent and process than integer?(CSE May/June 2007)**

An integer value requires only half the memory space as an equivalent.IEEEdouble-precision floatingpoint value. Applications that use only integer based arithmetic will therefore also have significantly smaller memory requirementA floating-point operation usually runs hundreds of times slower than an equivalent integer based arithmetic operation.

**19. .Give the booth's recoding and bit-pair recoding of the computer. 1000111101000101(CSE May/June 2006)**

Booth's recoding

1 0 0 0 1 1 1 1 0 1 0 0 0 1 0 1 0

-1 0 0 +1 0 0 0 -1 +1 -1 0 0 +1 -1 +1 -1

Bit-Pair recoding:

1 0 0 0 1 1 1 1 0 1 0 0 0 1 0 1 0
-2 +1 0 -1 +1 0 +1 1

**20. List out the rules for add/sub of floating point number?**

- Choose the number with the smaller exponent and shift its mantissa right a Number of steps equal to the difference in exponents.
- Set the exponent of the result equal to the larger exponent.
- Perform addition /subtraction on the mantissa and determine the sign of the Result.
- Normalize the resulting value, if necessary.

## PART-B

1 i).Discuss the multiplication algorithm its hardware and its sequential version with diagram. ii).Express the steps to Multiply 2*3. (6) (7) (Nov/Dec 2019)

2 Illustrate the multiplication of signed numbers using Booth algorithm. A=(-34)10=(1011110)2 and B=(22)10=(0010110)2 where B is multiplicand and A is multiplier. (13)

3 .Describe about basic concepts of ALU design. (13)

4. Develop algorithm to implement A*B. Assume A and B for a pair of signed 2's complement numbers with values:A=010111,B=101100 (13)

5 i).State the division algorithm with diagram and examples. ii).Divide 00000111 by 0010. (6) (7)

6. i).Express in detail about Carry looks ahead Adder. ii).Divide(12)10by(3)10 (8) (7)

7 .Point out how ALU performs division with flow chart and block diagram.(13)

8 i).Examine with a neat block diagram how floating point addition is carried out in a computer system. ii).Give an example for a binary floating point addition. (10) (3)

9 .What are the rules to perform addition on floating point numbers?(13)(Nov/Dec 2019)

10 State and explain the rules in arithmetic operation on floating point numbers. (NOV/DEC-2011)

# UNIT-3 THE PROCESSOR AND CONTROL UNIT

## PART A

**1. Define processor clock. (Nov/Dec 2019)**

The shortest time any computer is capable of performing is oneclock, or one vibration of the clock chip. The speed of acomputer processor is measured in clock speed, for example, 1 MHz is one million cycles, or vibrations, a second. 2 GHz is two billion cycles, or vibrations, a second

**2. What is imprecise and precise exception? (Nov/Dec 2019)**

imprecise exception. Asynchronous exception that does not adhere to the precise exception model. In the Cell Broadband Engine, single-precision floating-point operations generate imprecise exceptions. See also precise exception.

3. **Explain latency and throughput.**

Latency : Each Instruction takes certain amount of time to complete. This is called As latency. It is the time differences when an instruction is issued and when it is Completed.

Throughput : The number of instructions completed in a given time is called Throughput.

4. **What are the various stages in a pipeling execution**.
   - Instruction Fetch
   - Instruction Decode
   - Operand fetch
   - Opcode Execution
   - Write back
5. **What are Hazards?**

A hazard is also called as hurdle .The situation that prevents the next Instruction in the instruction stream from executing during its designated Clock Cycle. Stall is introduced by hazard. (Ideal stage)

6. **Define pipeline.**

A pipelining may be visualized as a collection of segments called pipe stages Through which binary information flows. Each segment performs partial processing As dictated by the task. The result obtained in each segment is transferred to the Next segment in the pipeline. The final result is obtained after the data passes Through all the segments.

7. **Explain latency and throughput.**

Latency : Each Instruction takes certain amount of time to complete. This is called As latency. It is the time differences when an instruction is issued and when it is Completed. Throughput : The number of instructions completed in a given time is called Throughput.

8. **What are the major characteristics of a pipeline?**
   - Pipelining cannot be implemented in a single task. As it works by splitting Multiple task into a number of subtask and operating on them simultaneously.
   - The speedup or efficicenty is achieved by using the pipelining depends on the Number of pipe stages and the number of available task that can be subdivide.
9. **What is a pipe stage?**

Each step in a pipeline is called as a pipe stage

10. **What is instruction pipeline?**

The type of pipeline which works by partitioning the instruction execution.

11. **What are the various stages in a pipeling execution.**
    - Instruction Fetch
    - Instruction Decode
    - Operand fetch
    - Opcode Execution
    - Write back
12. **Define Pipeline Hazards?**

The pipeline architectures works smoothly as long as it is able to take up new task In every machine cycle. In practice there are suitaution when the next instruction Can be executed in the following machine cycle. These events called as pipeline Hazards.

**13. State different types of hazards that can occur in pipeline.**

The types of hazards that can occur in the pipelining were,

- Data hazards.
- Instruction hazards.
- Structural hazards.

**14. Define Data hazards.**

Data hazards: A data hazard is any condition in which either the source or the destination Operands of an instruction are not available at the time expected in pipeline. As a Result some operation has to be delayed, and the pipeline stalls.

**15. Define Instruction hazards.**

Instruction hazards: The pipeline may be stalled because of a delay in the availability of an instruction.

For example, this may be a result of miss in cache, requiring the instruction to be Fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.

**16. Define Structural hazards.**

Structural hazards: The structural hazards is the situation when two instructions require the use of a Given hardware resource at the same time. The most common case in which this Hazard may arise is access to memory.

**17. What is superscalar processor?**

Super scalar processor exploits parallelism which has Multiple E_ Unit each of Which is pipelined and it constitutes independent Instruction pipeline. The processor Has PCU designed to fetch and decode several instructions concurrently which is Issued to pipeline E_Units that Executes several instruction is the same.

**18. What do you mean by out-of order execution? Is it Desirable?**

In a pipelined processor with several instructions is process concurrently it is Possible for instruction to finish out of sequence, one instruction finishes before Another which is issued earlier. As for as main computation is concerned no Hazards will happen but if an interrupts occurs it creates the problem.

**19. What are Hazards?**

A hazard is also called as hurdle .The situation that prevents the next Instruction in the instruction stream from executing during its designated Clock Cycle. Stall is introduced by hazard. (Ideal stage)

**20. List out Various branching technique used in micro program control Unit?**

- Bit-Oring

- Using Conditional Variable
- Wide Branch Addressing

## PART-B

1. Discuss the basics of logic design conventions. (13)

2. i) State the MIPS implementation in detail with necessary multiplexers and control lines. ii) Examine and draw a simple MIPS datapath with the control unit and the execution of ALU instructions. (7) (6)

3. i).Define parallelism and its types.

ii).List the main characteristics and limitations of Instruction level parallelism. (3) (10)

4 .Design and develop an instruction pipeline working under various situations of pipeline stall. (13) (MAY/JUNE-2013) ( APRIL/MAY-2010) ( MAY/JUNE-2011)

5 .i).What is data hazard? ii). Explain stalls with neat diagrams and suitable examples. (3) (10) (NOV/DEC-2011) ( APRIL/MAY-2010)

6 .Name and explain the two approaches used for generating the control signals in proper sequence.Differentiate the approaches (13) (Nov/Dec 2019)

7 .i).Differentiate sequential execution and pipelining. ii). Explain the process of building single data path with neat diagram. (3) (10)

8.Explain address translation method in virtual memory.( MAY/JUNE-2013)

9 .List the reason of pipeline conflicts in piplined processor.How are they resolved? (13) (Nov/Dec 2019)

10. i).Analyze the hazards caused by unconditional branching statements and pipelining a processor using an example. ii).Describe operand forwarding in a pipeline processor with a diagram. (7)(6)

## UNIT-4 PARALLELISM, MEMORY AND I/O SYSTEMS

## PART A

1. **Name the interconnections used in a multiprocessor system. (Nov/Dec 2019)**

   One type of interconnect topology is called a crossbar. A crossbar has every node of the network connected to every other node. Because any node can send simultaneous messages to every other node in the system without conflicts, this network topology is nonblocking.

2. **What is meant by hardware multithreading? (Nov/Dec 2019)**

Multi-Threading Models. Multithreading allows the execution of multiple parts of a program at the same time. These parts are known as threads and are lightweight processes available within the process. Therefore, multithreading leads to maximum utilization of the CPU by multitasking.

3. **Mention the group of lines in the system bus?**
   - Address lines
   - Data lines
   - Control lines
4. **What is DMA?**

   The CPU and IO controller interact only when the cpu yield the control of the memory bus to the IO controller in response to the request from the latter. This level of IO control is called direct memory access and IO device interface control circuit is called DMA controller.

5. **What is the use of IO controller?**

   The magnetic disks and other secondary memory need to be connected to the system bus via interface circuits called Io controllers. That performs series to parallel and parallel to series format conversions and other control functions. It can interface many IO device to system bus.

6. **What is bus master and slave master?**

   Input output operations involve data transfers between IO device and memory. In all the preceding operations memory is passive or slave device with respect to system bus transactions. Where as the cpu can control the system bus,i.e serve as a bus master.

7. **Differentiate synchronous and asynchronous communication?**

   In synchronous communication each item is transferred during the time slot know to both the source and destination. Data transfer is slow. In asynchronous communication data transfer is faster and can be used for long distance communication. Each item being transferred is accompanied by the control signals.

8. **What is strobe signal?**

   The data ready/request signals are used to load data from the source unit to the bus of from the bus to the destination unit.such control signals are called strobe signals.

9. **What is bus arbitration?**

   The possibility exists that several master or slave units connected to a shared bus will request access to the bus at the same time.A selection mechanism called bus arbitration is therefore required to enable the current master which will still refer to a bus controller to decide among such competing request.

10. **Mention the types of bus arbitration?**
    - Daisy chaining
    - Polling
    - Independent requesting
11. **What is IO control method?**

It refers the data transfer between the IO device and the memory or between the IO device and the cpu.eg.testing the ststus of device and to determine if they are required service by the cpu.

**12. What are the advantage and disadvantages of bus?**

ADV: 1.Low cost, 2.Versatility.

DIS-ADV: 1.It creates a communication bottleneck, 2.Limiting the maximum I/O throughput and bandwidth limitation.

**13. What are the types of buses?**

Processor memory bus

I/O Buses

**14. what are the i/o data transfer method using memory busses**

Three methods used for data transfer between io devices and cpu

- program i/o or polling
- interrupt driven i/o
- direct memory access

**15. Differentiate synchronous and asynchronous communication**.

In Synchronous communication each item is transferred during the time slot known to both source and destination Data transfer is slow In Asynchronous communication data transfer is faster and can be used for long distance communication. Each item being transferred accompanied by the control signals.

**16. How the interrupt is handled during exception?**

- cpu identifies source of interrupt
- cpu obtains memory address of interrupt handles
- HYPERLINK "http://www.indiastudychannel.com/resources/12626-CS--Computer-
- Architecture-Two-marks.aspx" \t "_top"pc and other cpu status information are
- saved
- Pc is loaded with address of interrupt handler and handling program to handle it.

**17. What is Full-HandShake**

A change of state in one signal is followed by a change in other signal. It provides the highest degree of flexibility and reliability.

**18. What is interrupt latency?**

Saving register also increases the delay between the time and interrupt request is received and state of execution of the interrupt service routine. This delay is called interrupt Latency.

**19. Define Centralized Arbitration.**

It means that all devices waiting to use the bus have no equal responsibility in carrying out the arbitration process.

**20. Define Distributed Arbitration.**

It means that all devices waiting to use the bus have equal responsibility in carrying out the arbitration process without using central arbiter.

## PART-B

1 i).Define parallelism and its types. ii).List the main characteristics and limitations of Instruction level parallelism. (4)(9)

2 i).Give the software and hardware techniques to achieve Instruction level parallelism. ii).Summarize the facts or challenges faced by parallel processing in enhancing computer architecture.(4)(9)

3 Express in detail about hardware multithreading. (13) (APRIL/MAY-2010)

4 Apply your knowledge on graphics processing units and explain how it helps computer to improve processor performance. (13) (Nov/Dec 2019)

5 Describe data level parallelism in i).SIMD. ii).MISD. (6) (7)

6 i).Point out how will you classify shared memory multi-processor based on memory access latency. ii).Compare and contrast Fine grained, Coarse grained multithreading and Simultaneous Multithreading. (7) (8)

7 Evaluate the features of Multicore processors. (13)

8 i).Classify the types of multithreading. ii).Analyze the advantages in multithreading. (9) (4)

9 Formulate the classes in Flynn's Taxonomy of computer Architecture classification with example. (13)

10 .explain in detail the shared memory multiprocessor, with the neat diagram(13) (Nov/Dec 2019)

## UNIT-5 PARALLEL COMPUTER ARCHITECTURES

## PARTA

1. **Define hit ratio. (Nov/Dec 2019)**

   The hit ratio is the number of hits divided by the total number of requests

2. **Differentiate USB and firewire. (Nov/Dec 2019)**

   The main difference between the two is that FireWire is made to handle more data than USB, particularly audio and visual information. For example, a 2.0 USB can handle a data transfer rate of 480 Mbps, whereas an 800 FireWire can take on 800 Mbps.

3. **Define Static Memories and Dynamic Memories.**

   Memories that consist of circuits‟ capable of retaining their state as long as power is applied

Are known‟s static memories. In Dynamic Memories such cells do not retain their state Indefinitely.

**4. What is SRAM AND DRAM?**

SRAM: Static randam access memory. It tends to be faster they require no refreshing

DRAM: Dynamic random access memory. Data is stored in the form of charges. So

continuous refreshing is needed.

**5. What is cache memory?**

Memory word are stored in cache data memory and are grouped into small pages called cache blocks or line. The contents of the cache‟s data memory are thus copies of a set of main memory blocks.

**6. What is memory system?**

Every Computer contains several types of devices to store the instructions and data for Its operation. These storage devices plus the algorithm implements by hardware and software Needed to manage the stored information from the memory system of computer.

**7. Give the classification of memory**

- Cpu Register
- Main memory
- Secondary Memory
- Cache.

**8. What is read access time?**

A basic performance measure is the average time to read a fixed amount of information for Instance, one word form the memory. This parameter is called the read access time.

**9. Define RAM**

In storage location can be accessed in any order and access time is independent of the Location being accessed, the memory is termed as random access memory.

**10. What is ROM?**

Memories whose content cannot be altered online if they can be altered at all are read only memories.

**11. What are PROMs?**

Semi conductor ROMs whose contents can be changed offline-with some difficulties is called PROMs.

**12. What is volatile memory?**

A memory is volatile if the loss of power destroys the stored information. Information can be stored indefinitely in a volatile memory by providing battery backup or other means to maintain a continuous supply of power.

**13. What are the categories of memories,**

- SRAM
- DRAM

**14. What is flash memory.**

A recent semiconductor technology called flash memory of a same non-volatility as aPROM, but it can be done a bit at a time.

**15. Mention two system organization for caches**.

Two system organization for caches are

- look aside
- look through

**16. What is RAMBUS memory?**

The key feature of Rambus technology is a fast signaling method used to transfer information between chip using narrow bus.

**17. What is write-through protocol?**

For write operation,the cache location and the main memory location are updated simultaneously.

**18. Give the difference between EEPROM and Flash memory?**

The primary difference between EEPROM and flash memory is that flash restricts writes to multiple kilobytes blocks, increasing the memory capacity per chip by reducing area of control.

**19. Differences between cache memory and virtual memory**

- In caches, replacement is primarily controlled by the hardware. In VM, replacement is primarily controlled by the os.
- The Number of bits in the address determines the size of VM, where as cache size is independent of the address size.
- But there is only one class of cache.

**20. Uses of Virtual Memory.**

Protection: VM is often used to protect one program from others in the system

Base and Bounds: this method allows relocation. User processes cannot be allowed to change These registers, but the OS must be able to do so on a process switch.

## PART-B

1.i).Define parallelism and its types. ii).List the main characteristics and limitations of Instruction level parallelism. (7) (6)

2.i).Define virtual memory and its importance. ii).Examine TLB with necessary diagram .What is its use? (7) (6)

3 .i).List the various memory technologies and examine its relevance in architecture design. ii). Identify the characteristics of memory system. (7) (6)

4 .Apply how Internal Communication Methodologies is useful in developing computer architecture. (13)

5.i).Demonstrate the DMA controller. Discuss how it improves the overall performance of the system. ii).Illustrate how DMA controller is used for direct data transfer between memory and peripherals? (7) (6)

6. Point out the need for cache memory. Explain the following three mapping methods with examples. i). Direct. ii).Associative. iii).Set associative. (13)

7 .What is cache memory? What are the two ways in which the system using cache can proceed for a write operation? (13) (Nov/Dec 2019) (NOV/DEC-2011) (MAY/JUNE-2013) (APRIL/MAY-2010)

8 .Generalize the Bus Structure, Protocol, and Control in Parallel Bus Architecture (13) (MAY/JUNE-2011)

9 .i).Classify the types of memory chip organization. ii).Analyze the advantages of cache and virtual memory (7) (6) (Nov/Dec 2019)

10. Elaborate in detail about the following in Parallel Bus Architectures i). The Synchronous Bus ii). The Asynchronous Bus (7) (6)